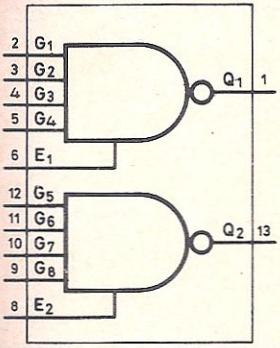
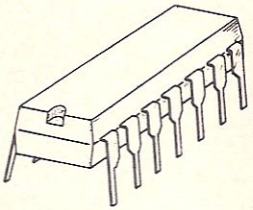
DUAL 4-INPUT LINE DRIVER NAND GATE

development sample data





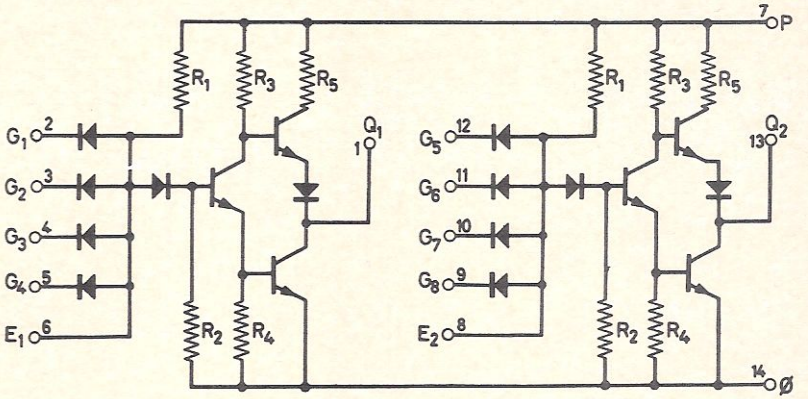
QUICK REFERENCE DATA

Supply voltage	V_P		6.0 ± 5%	V
Operating ambient temperature range	T_{amb}		0 to 75	°C
Average propagation delay time, at fan-out N = 20, C_W = 250 pF and T_{amb} = 25 °C	t_{pd}	max.	93	ns
Available d.c. fan-out at T_{amb} = 25 °C	N_a		20	
D.C. noise margin at T_{amb} = 25 °C	M_L	min.	0.6	V
		typ.	1.2	V
Power consumption per gate 50% duty cycle; T_{amb} = 25 °C	P_{av}	typ.	11	mW
Package		D1	(Dual in-line)	

The FCH231 comprises two independent NAND gates (positive logic) incorporating bi-directional output circuitry for achieving very high fan-out and driving large capacitive loads. Typical applications of the FCH231 include parallel setting of registers, shift pulse driving and driving long cables.

These data, based on the specifications and measured performance of development samples, afford a preliminary indication of the characteristics to be expected of the described product. Distribution of development samples implies no guarantee as to the subsequent availability of the product

CIRCUIT DIAGRAM



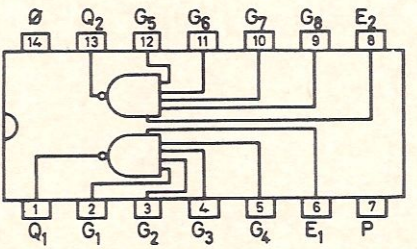
LOGIC FUNCTION

$Q_1 = \overline{G_1 . G_2 . G_3}$ (positive logic)

G_1	G_2	G_3	Q_1
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

H = HIGH state (the more positive signal voltage)
L = LOW state (the less positive signal voltage)

TERMINAL CONNECTIONS (Top view)



INTRODUCTION TO THE CHARACTERISTICS

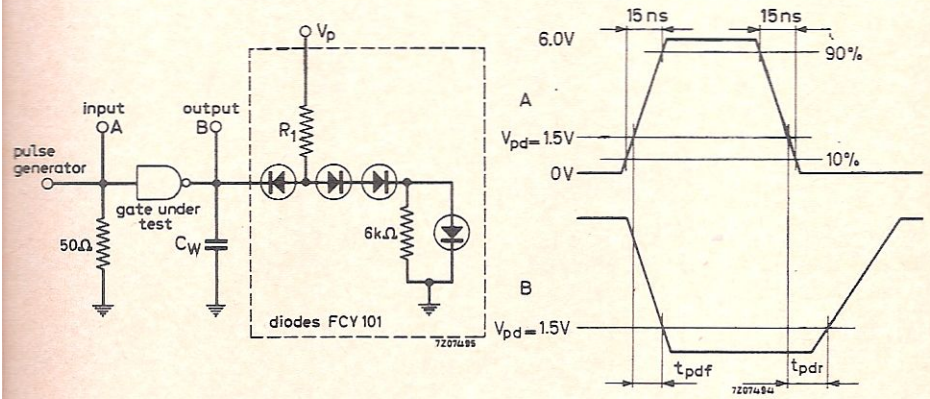
1. General assumptions

- All voltages are assumed to be measured with respect to the reference terminal, designated by ⏚.
- A current is taken as positive when its conventional direction of flow is into the device.
- Where no electrical conditions are specified for a given terminal, it is left unconnected.
- Conditions such as "Input V_{QLmax}" are to be understood as follows: for each temperature, the maximum value of the voltage V_{QL} is applied to the input.
- All values quoted apply to each individual gate.

2. Input threshold voltage levels V_{GL} and V_{GH}. Output current I_{QL}.

At input voltages equal to the threshold voltage levels V_{GL} and V_{GH}, the circuit is near the limit of switching.
I_{QL} is the value of LOW state output current at and below which V_Q will not exceed V_{QLmax}.
V_{GL}, V_{GH} and I_{QL} are defined as being independent of any condition except temperature, thus forming the basis of the other circuit variables.

3. Propagation delay time measurement N = number of loading gates.



Loading circuit, simulating load of N = 20 gates (FCH101 to 211)
R_1 = 180 Ω

INTRODUCTION TO THE CHARACTERISTICS (continued)

4. Fan-out and noise margins

Available fan-out and noise margins as specified under quoted conditions represent guaranteed limit values applicable to the entire supply voltage range from 5.7 to 6.3 V (the noise margins at any load between N=1 and $N=N_a$) provided that

a) driving and driven circuits are operating at the same ambient temperature and the same supply voltage;

b) in the LOW state, the sum of the diode leakage currents through inputs other than those driven directly by the gate concerned, may be neglected.

CHARACTERISTICS

	Electrical conditions				T_{amb} (°C)			
	input G	output Q	supply P		0	25	75	
STATIC DATA								
Input threshold voltage levels								
- input LOW	-	-	5.7 to 6.3 V	V_{GL}	1.0	1.0	0.8	V
- input HIGH	-	-	5.7 to 6.3 V	V_{GH}	2.3	2.2	2.1	V
Output voltage levels								
- output LOW	V_{GH}	I_{QL}	5.7 V	V_{QL} max.	0.4	0.4	0.4	V
- output HIGH, unloaded	V_{GL}	R to Ø / 1 MΩ	5.7 V	V_{QH} min.	3.5	3.7	4.0	V
- output HIGH, voltage drop with loading	V_{GL}	$-I_Q$ = a μA	5.7 V	ΔV_{QH} max.	a x 0.19	a x 0.19	a x 0.22	mV
Output current								
- output LOW	-	-	5.7 V	I_{QL}	35.0	36.3	31.5	mA
Input currents								
- input LOW	V_{QLmax}	-	5.7 V	$-I_{GL}$ max.	1.75	1.65	1.55	mA
			6.3 V	$-I_{GL}$ max.	2.0	1.9	1.8	mA
- input HIGH	V_{QHmin}; other inputs V_G = 0	-	5.7 V	I_{GH} max.	1.0	1.0	25	μA

CHARACTERISTICS (continued)

	supply P		T_{amb} (°C)			
			0	25	75	
DYNAMIC DATA						
Prop. delay reference level	–	V_{pd}	1.5	1.5	1.5	V
Rise propagation delay time N = 20; C_W = 250 pF	6.0 V	t_{pdr} max.	130	105	130	ns
Fall propagation delay time N = 20; C_W = 250 pF	6.0 V	t_{pdf} max.	95	80	95	ns
Input capacitance (equiv.)	6.0 V	C_G typ.		7		pF
SUPPLY CURRENT (per gate)						
- output LOW	6.0 V	I_{PL} typ.	2.3	2.35	2.3	mA
- output HIGH	6.0 V	I_{PH} typ.	1.3	1.25	1.2	mA
DERIVED DATA						
Available d.c. fan-out to similar circuits (uniform system supply voltage)	5.7 to 6.3 V	N_a	20	22	20	
D.C. noise margins to similar circuits						
- LOW	5.7 V	M_L min.	0.6	0.6	0.4	V
- HIGH	5.7 V	M_H min.	1.1	1.4	1.7	V
Average prop. delay time						
$\frac{t_{pdr} + t_{pdf}}{2}$ (N = 20; C_W = 250 pF)	6.0 V	t_{pd} max.	113	93	113	ns
Power supply consumption (per gate)						
50 % duty cycle	6.0 V	P_{av} typ.	11	11	10.5	mW

ADDITIONAL SYSTEM DESIGN DATA

Fan-out and noise margins related to NAND gates FCH101 to 211

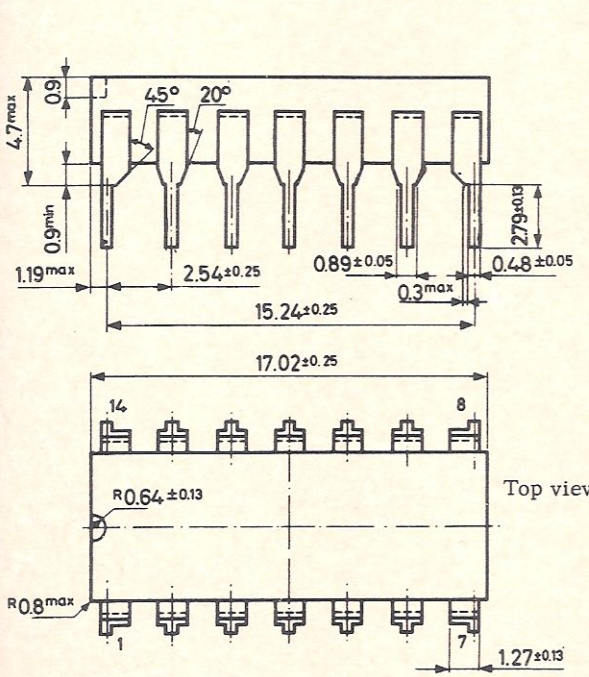
		supply P		T_{amb} (°C)			
				0	25	75	
Available d.c. fan-out to NAND gates (uniform system supply voltage)		5.7 to 6.3 V	N_a	20	22	20	
D.C. noise margins							
- from NAND gate to FCH231	LOW	5.7 V	M_L min.	0.6	0.6	0.4	V
	HIGH	5.7 V	M_H min.	2.9	3.0	1.8	V
- from FCH231 to NAND gate	LOW	5.7 V	M_L min.	0.6	0.6	0.4	V
	HIGH	5.7 V	M_H min.	1.1	1.4	1.7	V

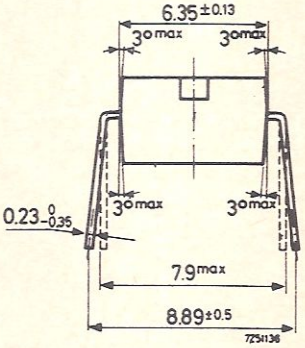
RATINGS (Limiting values [1])

Supply voltage	V_P	max.	8	V
Output voltage	V_Q	0 to	8	V
Input voltage	V_G	max.	8	V
Neg. input current	$-I_G$	max.	20	mA [2]
Storage temperature	T_{stg}	−35 to +125		°C
Operating ambient temperature	T_{amb}	0 to +75		°C

PACKAGE OUTLINE

Dimensions in mm



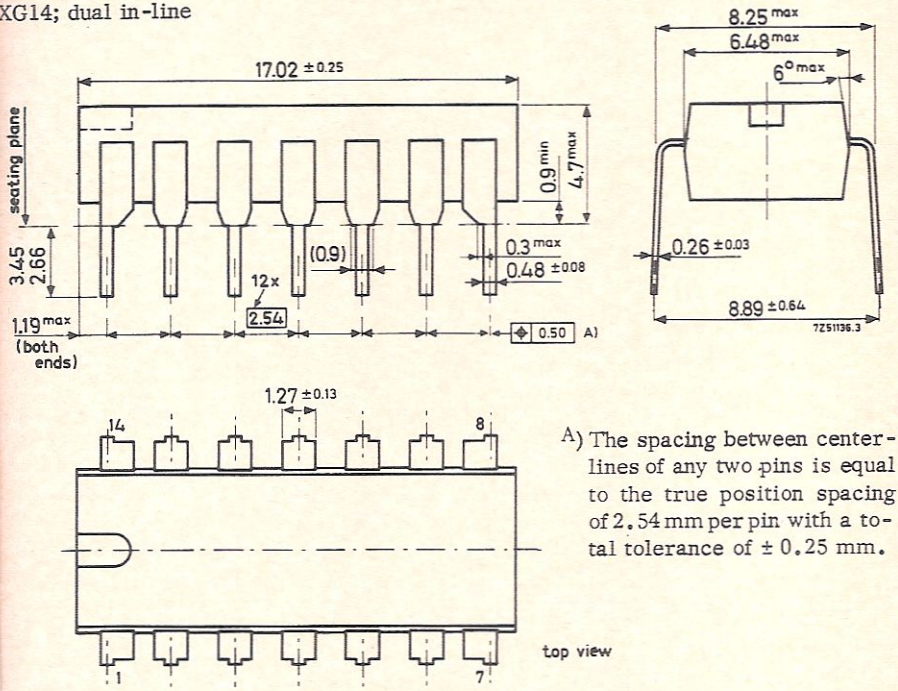


[1]) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.
[2]) At this limit $-V_G$ typ. 1.5 V.
[3]) Tolerance non-cumulative.

PACKAGE OUTLINE

XG14; dual in-line

Dimensions in mm



A) The spacing between centerlines of any two pins is equal to the true position spacing of 2.54 mm per pin with a total tolerance of ± 0.25 mm.

Handling notes

1. Devices may be soldered directly into circuits with soldering irons. At iron temperatures below 245 °C the maximum soldering time should be less than 10 seconds and at iron temperatures between 245 °C and 400 °C the soldering time should be less than 5 seconds. In both cases the soldering iron should be applied below the seating plane (see outline drawing).

2. Devices mounted up to the seating plane on a printed circuit board may be dip or flow soldered providing the solder temperature is below 245 °C and the time of immersion is less than 5 seconds. The body temperature should not be allowed to exceed the maximum storage temperature during soldering. If excessive preheat cycles are used, it may be necessary to cool the printed board immediately after leaving the solder bath/wave in order that this requirement is met.